CLAIMS:

1. A device comprising a processing circuit (B1; B1, B11) with a predetermined limited dynamic range, and an automatic gain control circuit comprising:

a gain determining circuit (B2) for determining a first gain factor (g),

a first gain controller (B3) for controlling an amplitude of an input signal (S1) with the first gain factor (g) to supply a gain controlled signal (S3) to the processing circuit (B1; B1, B11),

a compensation circuit (B5) for determining a second gain factor (dg) based on the first gain factor (g) and input parameters (DL, TR, DV) defining a time variation of the second gain factor (dg), and

a second gain controller (B1; B10) for receiving an output signal of the processing circuit (B1; B1, B11) and the second gain factor (dg) to obtain a compensated output signal (S2) being substantially compensated for an amplitude change of the gain controlled signal (S3) due to a change of the first gain factor (g).

2. A device as claimed in claim 1, wherein the processing circuit (B1; B1, B11) comprises an analog to digital converter (B1) for converting the gain controlled signal (S3) into a digital signal (S4; S2), the output signal of the processing circuit (B1; B1, B11) being a digital signal (S4), and the compensated output signal (S2) being a compensated digital signal (S2).

3. A device as claimed in claim 2, wherein the gain determining circuit (B2) has inputs for receiving the gain controlled signal (S3) and/or the digital signal (S4) and an output for supplying the first gain factor (g), the first gain factor (g) being determined to obtain the amplitude of the gain controlled signal (S3) fitting within an operating range of the analog to digital converter (B1).

4. A device as claimed in claim 3, wherein the gain determining circuit (B2) is arranged for adapting the first gain factor (g) in steps.

5. A device as claimed in claim 4, wherein the steps comprise powers of the number two.

6. A device as claimed in claim 1, wherein the compensation circuit (B5) comprises a delay circuit (B6) for delaying a start instant of a change of the second gain factor (dg) in response to the change of the first gain factor (g) to substantially compensate for a processing time of the processing circuit (B1; B1, B11) causing a time delay (TD) between the gain controlled signal (S3) and the compensated output signal (S2).

7. A device as claimed in claim 1, wherein the compensation circuit (B5) comprises a waveform generating circuit (B7) for generating a waveform (WF) of the time variation of the second gain factor (dg).

8. A device as claimed in claim 7, wherein the waveform generating circuit (B7) comprises a bandwidth limitation circuit, or a linear interpolation circuit, or a higher order interpolation circuit, or a table look up circuit, or a line drawing algorithm circuit.

9. A device as claimed in claim 1, wherein the compensation circuit (B5) comprises a level adaptating circuit (B8) for generating a DC-offset of the second gain factor (dg) to substantially compensate for a static level deviation (E) of the compensated output signal (S2).

10. A device as claimed in claim 2, wherein the analog to digital converter (B1) is of a single bit sigma-delta type.

11. A device as claimed in claim 2, wherein the analog to digital converter (B1) comprises the second gain controller (B1; B10) for controlling the gain of the digital signal (S4) to supply the compensated digital signal (S2).

12. A device as claimed in claim 2, wherein the second gain controller (B1; B10) is arranged for controlling the gain of the digital signal (S4) supplied by the analog to digital converter (B1).

13. A device as claimed in claim 2, wherein the processing circuit (B1; B1, B11) comprises a digital processing circuit (B11) for processing the digital signal (S4) supplied by the analog to digital converter (B1) to obtain a processed digital signal (S5), and wherein the second gain controller (B10) is arranged for controlling a gain of the processed digital signal (S5) with the second gain factor (dg).

14. A device as claimed in claim 13, further comprising a digital gain controller (B12) being arranged between the analog to digital converter (B1) and the digital processing circuit (B11), the digital gain controller (B12) being controlled by a further digital gain factor (dga).

15. A device as claimed in claim 1, further comprising an automatic calibration circuit (B13) being arranged for, during a test period (TP), repeatedly:

generating a reference signal (RS) being supplied as the input signal (S1),

adapting the first gain factor (g) with a predetermined amount,

providing a first set of input parameters (DL, TR, DV),

checking whether a change of amplitude occurs of the compensated output signal (S2), and

adapting at least one of the input parameters (DL, TR, DV), until substantially no change of amplitude occurs of the compensated output signal (S2), and

finally storing the input parameters (DL, TR, DV) determined, for use during normal operation.

16. A method of automatic gain control in a device comprising a processing circuit (B1; B1, B11) with a predetermined limited dynamic range, the method comprising:

determining (B2) a first gain factor (g),

controlling (B3) an amplitude of an input signal (S1) with the first gain factor (g) to supply a gain controlled signal (S3) to the processing circuit (B1; B1, B11),

determining (B5) a second gain factor (dg) based on the first gain factor (g) and input parameters (DL, TR, DV) defining a time variation of the second gain factor (dg), and

controlling (B1; B10) with the second gain factor (dg) an output signal of the processing circuit (B1; B1, B11) to obtain a compensated output signal (S2) being

substantially compensated for an amplitude change of the gain controlled signal (S3) due to a change of the first gain factor (g).

17. A method of automatic gain control as claimed in claim 16, further comprising an automatic calibration (B13) comprising, during a test period, repeatedly:

generating a reference signal (RS) being supplied as the input signal (S1),

adapting the first gain factor (g) with a predetermined amount,

providing a first set of input parameters (DL, TR, DV),

checking whether a change of amplitude occurs of the compensated output signal (S2), and

adapting at least one of the input parameters (DL, TR, DV), until substantially no change of amplitude occurs of the compensated output signal (S2), and

finally storing the input parameters (DL, TR, DV) determined, for use during normal operation.

18. An audio apparatus comprising a processing circuit (B1; B1, B11) with a predetermined limited dynamic range, and an automatic gain control circuit comprising:

a gain determining circuit (B2) for determining a first gain factor (g),

a first gain controller (B3) for controlling an amplitude of an input signal (S1) with the first gain factor (g) to supply a gain controlled signal (S3) to the processing circuit (B1; B1, B11),

a compensation circuit (B5) for determining a second gain factor (dg) based on the first gain factor (g) and input parameters (DL, TR, DV) defining a time variation of the second gain factor (dg), and

a second gain controller (B1; B10) for receiving an output signal of the processing circuit (B1; B1, B11) and the second gain factor (dg) to obtain a compensated output signal (S2) being substantially compensated for an amplitude change of the gain controlled signal (S3) due to a change of the first gain factor (g).